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iddq <and> processor <and> fault

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JNL = Journal or Magazine **CNF** = Conference **STD** = Standard**1 Current sensor and test processor design for integration of logic and IDDQ testing of CMOS ICs***Altaf-Ul-Amin, M.; Darus, Z.M.;*

Semiconductor Electronics, 1998. Proceedings. ICSE '98. 1998 IEEE

International Conference on , 24-26 Nov. 1998

Pages:162 - 167

[\[Abstract\]](#) [\[PDF Full-Text \(464 KB\)\]](#) **IEEE CNF****2 Proceedings the European Design and Test Conference. ED&TC 1995**

European Design and Test Conference, 1995. ED&TC 1995, Proceedings. , 6-9

March 1995

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1 [Atomic snapshots in \$O\(n \log n\)\$ operations](#)

Hagit Attiya, Ophir Rachman

September 1993

Proceedings of the twelfth annual ACM symposium on Principles of distributed computing

Full text available:  [pdf\(1.22 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [Fault-tolerance in the advanced automation system](#)

Flaviu Cristian, Bob Dancey, Jon Dehn

September 1990

Proceedings of the 4th workshop on ACM SIGOPS European workshop

Full text available:  [pdf\(1.39 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


The Advanced Automation System is a distributed real-time system under development by IBM's Systems Integration Division for the US Federal Aviation Administration. The system is intended to replace the present en-route and terminal approach US air traffic control computer systems over the next decade. High availability of air traffic control services is an essential requirement of the system. This paper discusses the general approach to fault-tolerance adopted in AAS, by reviewing some of the q ...

3 [Understanding fault-tolerant distributed systems](#)

Flavin Cristian

February 1991

Communications of the ACM, Volume 34 Issue 2

Full text available:  [pdf\(6.17 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#), [review](#)

4 [A fault diagnosis methodology for the UltraSPARC/sup TM/-I microprocessor](#)

S. Narayanan, R. Srinivasan, R. P. Kunda, M. E. Levitt, S. Bozorgui-Nesbat

March 1997

Proceedings of the 1997 European conference on Design and Test

Full text available:  [pdf\(900.08](#)

[KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#)

In this paper we study the use of precomputed fault dictionaries to diagnose stuck-at and bridging defects in the UltraSPARC/sup TM/-I processor. In constructing the dictionary we analyze the effect of the dictionary format on parameters such as memory size, computational effort, and diagnostic resolution. The dictionary is built based on modeled stuck-at faults. However to effectively diagnose both stuck-at and bridging faults, we employ a novel procedure that

combines dictionary information wi ...

Keywords: UltraSPARC-I microprocessor, bridging defects, computational effort, computer testing, diagnostic resolution, failure mechanisms, fault diagnosis methodology, layout, memory size, precomputed fault dictionaries, predicted errors, stuck-at defects

5 Dynamic verification of operating system decisions

R. S. Fabry

November 1973 **Communications of the ACM**, Volume 16 Issue 11

Full text available:  [pdf\(1.09 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)


Dynamic verification of a decision implies that every time the decision is made there is a consistency check performed on the decision using independent hardware and software. The dynamic verification of operating system decisions is used on the PRIME system being designed and constructed at the University of California, Berkeley. PRIME is an experimental time-sharing system which is to have the properties of continuous availability, data privacy, and cost effectiveness. The technique of dy ...

Keywords: data privacy, data security, fault tolerance, modular computer systems, operating systems, program verification, software reliability

6 Mark IIIfp hypercube concurrent processor architecture

J. Tuazon, J. Peterson, M. Pniel

January 1988 **Proceedings of the third conference on Hypercube concurrent computers and applications: Architecture, software, computer systems, and general issues - Volume 1**

Full text available:  [pdf\(1.02 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The Mark IIIfp Hypercube is a new generation of hypercube concurrent processor system developed at JPL/Caltech, with peak performance of 5 Mips, 14 Mflops per node, and a peak communication rate of 6 Mbytes per second. Each node utilizes two Motorola MC68020 microprocessors, an MC68882 scalar floating-point coprocessor, and a Weitek 8000 floating-point chip set. One of the MC68020 processors serves as the application and computational processor, the other is dedicated to communication. The ...

7 Demonstrable fault tolerance for distributed Ada

Pat Rogers, Steve O'Neill, Marc Pitarys, Ken Littlejohn


October 1993 **Proceedings of the conference on TRI-Ada '93**

Full text available:  [pdf\(931.99 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

8 Emerging areas: Fault-tolerant platforms for automotive safety-critical applications

M. Baleani, A. Ferrari, L. Mangeruca, A. Sangiovanni-Vincentelli, Maurizio Peri, Saverio Pezzini

October 2003 **Proceedings of the international conference on Compilers, architectures and synthesis for embedded systems**

Full text available:  [pdf\(736.40 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Fault-tolerant electronic sub-systems are becoming a standard requirement in the automotive industrial sector as electronics becomes pervasive in present cars. We address the issue of fault tolerant chip architectures for automotive applications. We begin by reviewing fault-tolerant architectures commonly used in other industrial domains where fault-tolerant electronics has been a must for a number of


years, e.g., the aircraft manufacturing industrial sector. We then proceed to investigate how t ...

Keywords: VLSI, automotive, fault-tolerant, multi-processor, safety critical, system-on-a-chip

9 The TickerTAIP parallel RAID architecture

Pei Cao, Swee Boon Lin, Shivakumar Venkataraman, John Wilkes

August 1994 **ACM Transactions on Computer Systems (TOCS)**, Volume 12 Issue 3

Full text available:  [pdf\(2.04 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Traditional disk arrays have a centralized architecture, with a single controller through which all requests flow. Such a controller is a single point of failure, and its performance limits the maximum number of disks to which the array can scale. We describe TickerTAIP, a parallel architecture for disk arrays that distributes the controller functions across several loosely coupled processors. The result is better scalability, fault tolerance, and flexibility. This article presents ...

Keywords: RAID disk array, decentralized parity calculation, disk scheduling, distributed controller, fault tolerance, parallel controller, performance simulation

10 Distributed systems - programming and management: On remote procedure call

Patrícia Gomes Soares

November 1992 **Proceedings of the 1992 conference of the Centre for Advanced Studies on Collaborative research - Volume 2**

Full text available:  [pdf\(4.52 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for the future ...

11 Fault tolerant distributed services

Allan D. Grier, H. Raymond Strong


January 2000 **Proceedings of the seventh annual ACM Symposium on Principles of distributed computing**

Full text available:  [pdf\(1.12 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

12 Preserving and using context information in interprocess communication

Larry L. Peterson, Nick C. Buchholz, Richard D. Schlichting


August 1989 **ACM Transactions on Computer Systems (TOCS)**, Volume 7 Issue 3

Full text available:  [pdf\(2.47 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

When processes in a network communicate, the messages they exchange define a partial ordering of externally visible events. While the significance of this partial order in distributed computing is well understood, it has not been made an explicit part of the communication substrate upon which distributed programs are implemented. This paper describes a new interprocess communication mechanism, called Psync, that explicitly encodes this partial ordering with each message. The ...

13 The transport layer: tutorial and survey

Sami Iren, Paul D. Amer, Phillip T. Conrad


Full text available:  [pdf\(261.78 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Transport layer protocols provide for end-to-end communication between two or more hosts. This paper presents a tutorial on transport layer concepts and terminology, and a survey of transport layer services and protocols. The transport layer protocol TCP is used as a reference point, and compared and contrasted with nineteen other protocols designed over the past two decades. The service and protocol features of twelve of the most important protocols are summarized in both text and tables.< ...

Keywords: TCP/IP networks, congestion control, flow control, transport protocol, transport service

14 Scheduler-conscious synchronization

Leonidas I. Kontothanassis, Robert W. Wisniewski, Michael L. Scott
February 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 1


Full text available:  [pdf\(682.20 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Efficient synchronization is important for achieving good performance in parallel programs, especially on large-scale multiprocessors. Most synchronization algorithms have been designed to run on a dedicated machine, with one application process per processor, and can suffer serious performance degradation in the presence of multiprogramming. Problems arise when running processes block or, worse, busy-wait for action on the part of a process that the scheduler has chosen not to run. We show ...

Keywords: barriers, busy-waiting, kernel-user interaction, locks, mutual exclusion, preemption, scalability, scheduling, synchronization

15 Unbounded speed variability in distributed communication systems



John Reif, Paul Spirakis
January 1982 **Proceedings of the 9th ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

Full text available:  [pdf\(978.22 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

This paper concerns the fundamental problem of synchronizing communication between distributed processes whose speeds (steps per real time unit) vary dynamically. Communication must be established in matching pairs, which are mutually willing to communicate. We show how to implement a distributed local scheduler to find these pairs. The only means of synchronization are boolean "flag" variables, each of which can be written by only one process and read by at most one other process. No global boun ...

16 Power and performance evaluation of globally asynchronous locally synchronous processors

Anoop Iyer, Diana Marculescu
May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2

Full text available:  [pdf\(1.10 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)
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Due to shrinking technologies and increasing design sizes, it is becoming more difficult and expensive to distribute a global clock signal with low skew throughout a processor die. Asynchronous processor designs do not suffer from this problem since they do not have a global clock. However, a paradigm shift from synchronous to asynchronous is unlikely to happen in the processor industry in the near future. Hence the study of Globally Asynchronous Locally Synchronous (or GALS) systems is relevant ...

17 A flat, timing-driven design system for a high-performance CMOS processor chipset

J. Koehl, U. Baur, T. Ludwig, B. Kick, T. Pflueger

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available:  [pdf\(155.54](#)

[KB\)](#)  [Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We describe the methodology used for the design of the CMOS processor chipset used in the IBM S/390 Parallel Enterprise Server - Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm² is comparable to the most advanced custom designs and that the impact of interconnect d ...

18 On reliable message diffusion

Y. Moses, G. Roth


June 1989 **Proceedings of the eighth annual ACM Symposium on Principles of distributed computing**

Full text available:  [pdf\(1.09 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

19 Efficient at-most-once messages based on synchronized clocks

Barbara Liskov, Liuba Shrira, John Wroclawski

May 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 2

Full text available:  [pdf\(1.33 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

This paper describes a new at-most-once message passing protocol that provides guaranteed detection of duplicate messages even when the receiver has no state stored for the sender. It also discusses how to use at-most-once messages to implement higher-level primitives such as at-once-remote procedure calls and sequenced bytestream protocols. Our performance measurements indicate that at-most-once RPCs can provide at the same cost as less desirable forms of RPCs that do not guarantee at-mos ...

Keywords: at-most-once message passing, message-passing protocols, remote procedure calls, synchronized clocks

20 Integrating security in a large distributed system

M. Satyanarayanan

August 1989 **ACM Transactions on Computer Systems (TOCS)**, Volume 7 Issue 3

Full text available:  [pdf\(2.90 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Andrew is a distributed computing environment that is a synthesis of the personal computing and timesharing paradigms. When mature, it is expected to encompass over 5,000 workstations spanning the Carnegie Mellon University campus. This paper examines the security issues that arise in such an environment and describes the mechanisms that have been developed to address them. These mechanisms include the logical and physical separation of servers and clients, support for secure communication ...

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